CLAIMS:

1. A frequency divider circuit comprising:

an even number of amplifier stages connected in series with the output of the last amplifier stage connected to the input of the first amplifier stage; and

modulating means, responsive to an input signal to be frequency divided, for modulating the propagation delay through each of said amplifier stages, about the period of the input signal to be divided, such that when the propagation delay through the odd amplifier stage(s) increases, the propagation delay through the even amplifier stage(s) decreases.

2. A frequency divider circuit according to claim 1, wherein there are two amplifier stages connected in series.

3. A frequency divider circuit comprising a plurality of frequency divider circuits according to claim 1 or 2 connected in series.

4. A frequency divider circuit according to claim 1, 2 or 3, wherein each amplifier is a differential amplifier.

5. A frequency divider circuit according to any preceding claim, wherein each amplifier stage comprises an amplifier with hysteresis.

6. A frequency divider circuit according to any preceding claim, wherein said modulating means varies the strength of connection between adjacent amplifier stages.

7. A frequency divider circuit according to claim 5,

wherein said modulating means varies the hysteresis of each of said amplifier stages.

8. A frequency divider circuit according to any preceding claim, wherein said frequency divider circuit is a FET type semiconductor circuit.

9. A frequency divider circuit according to claim 8, integrated monolithically with complementary FET logic.

10. A frequency divider circuit according to claim 8, wherein said frequency divider circuit is a CMOS circuit integrated monolithically with CMOS logic circuitry in a standard CMOS process.

11. A frequency divider circuit according to any preceding claim, suitable for use where the frequency of the input signal to be divided is greater than 100 MHz.

12. A frequency divider circuit according to any preceding claim, further comprising logic means for providing dividing by ratios other than simple powers of two.

13. A frequency divider circuit according to any preceding claim, wherein each of said amplifier stages comprises a latch circuit having two inverters connected in a memory arrangement with the output of one connected to the input of the other.

14. A semiconductor latch comprising:
a data input;
a data output;
a clock input;
two inverters connected in a memory arrangement with

the output of one connected to the input of the other; and

input means connected to said memory arrangement, for writing new data applied to said data input into said memory arrangement, in dependence upon a clock signal applied to said clock input;

characterised in that

said latch comprises varying means for varying the time taken for new data to be written into said memory arrangement.

15. A semiconductor latch according to claim 14, wherein said varying means varies the strength of connection between said input means and said memory arrangement.

16. A semiconductor latch according to claim 14, wherein said varying means varies the hysteresis of the memory arrangement.

17. A semiconductor latch according to claim 14, 15 or 16, wherein said latch is a FET type latch in an integrated circuit.

18. A semiconductor latch according to claim 17, wherein said latch is a CMOS latch in an integrated circuit.

19. A semiconductor latch according to any of claims 13 to 18, wherein said varying means varies the time taken for new data to be written into said memory arrangement in response to a clock signal applied to said clock input.

20. A method of frequency division using an even number of amplifier stages connected in series with the output of the last amplifier stage connected to the input of the

first amplifier stage, the method comprising:

modulating the propagation delay through each of said amplifier stages, about the period of the input signal to be divided, such that when the propagation delay through odd-numbered amplifier stage(s) increases, the propagation delay through even-numbered amplifier stage(s) decreases.

21. A method according to claim 20, wherein each amplifier is a differential amplifier.

22. A method according to claim 20 or 21, wherein each amplifier stage used comprises an amplifier with hysteresis.

23. A method according to claim 20, 21 or 22, wherein said modulating step varies the strength of connection between adjacent amplifier stages.

24. A method according to claim 22, wherein said modulating step varies the hysteresis of each of said amplifier stages.

25. A method according to any of claims 20 to 24, wherein said amplifier stages comprise an FET type semiconductor integrated circuit.

26. A method according to claim 25, wherein said amplifier stages comprise a CMOS integrated circuit.

27. A method according to any of claims 20 to 26, wherein the frequency of the input signal to be divided is greater than 100 MHz.

28. A method according to any of claims 20-27, wherein

said method also uses logic circuits for providing division by ratios other than simple powers of two.

29. A radio receiver comprising a frequency divider circuit according to any of claims 1 to 12 or utilising a method of frequency division according to any of claims 20 to 28.

30. A radio receiver comprising a latch circuit according to any of claims 13 to 19.